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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,511	MARTINEZ, ANTONIO MARROIG	
	Examiner	Art Unit	
	John P. Trimmings	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-24 are presented for examination.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because FIG.2 fails to show connections between the Comparator 52 and both the Receive and Transmit Registers as described in the specification. A connection, such as a line of communication, should be added to the drawing in order to more clearly depict the internal structure of the BIST.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: FIG.2 40.

3. The drawings are objected to because FIG.5 Array 104 contains an incomplete descriptor, "-bit by m-wor register array". The examiner requests that the descriptor be rearranged, re-worded, or removed in order to eliminate confusion.

4. The drawings are objected to because FIG.5 Control Logic 116 contains an incomplete line of connection between 116 and two registers 110 and 112. The examiner requests that the figure be corrected.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign mentioned in the description: FIG.5 110.

Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

6. The disclosure is objected to because of the following informalities:

Page 6 line 24 should be corrected to recite, "... to control line [~~44~~] 40 or ...".

Page 9 line 3 should be corrected to recite, "... internal busses [~~120~~] 122 or control signals [~~122~~] 120 ...".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear to the examiner whether the transmit register of line 3 transmits data to the serializer, deserializer, or both serializer and deserializer (also on line 3). The term, "serializer/deserializer" is known in the art to be two units (serializer and deserializer) integrated onto a single package. But when describing data flow, especially in a patent claim, it is common practice in the art to refer to the units separately in order to eliminate confusion. The serializer/deserialzer of line 6 also represents indefiniteness as to which unit is supplying "processed data" to the receive register.

8. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant

regards as the invention. The "processed data" of lines 5 and 7 cannot be the same "processed data" recited in line 4. One with ordinary skill in the art, after reading the Disclosure, would assume that the "processed data" of line 4 would be serial, and that the "processed data" of lines 5 and 7 are parallel, therefore the meaning of processed data in the claim is indefinite.

9. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The examiner, being one of ordinary skill, and after reading the Disclosure, is under the assumption that "the transmitted data" of Claim 1 line 3 is parallel data. Also, the "processed data" of Claim 1 line 4 is assumed to be serial data after reading the Disclosure. Therefore, the Claim 10 is indefinite when it recites the limitation, "the transmit data and processed data are parallel data".

10. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear to the examiner whether the transmit register of line 3 transmits data to the serializer, deserializer, or both serializer and deserializer (line 4). The term, "serializer/deserializer" is known in the art to be two units (serializer and deserializer) integrated onto a single package. But when describing data flow, especially in a patent claim, it is common practice in the art to refer to the units separately in order to eliminate confusion. The serializer/deserialzer of line 7 also

represents indefiniteness as to which unit is supplying "processed data" to the receive register.

11. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The "processed data" of lines 6 and 8 cannot be the same "processed data" recited in lines 4 and 5. One with ordinary skill in the art, after reading the Disclosure, would assume that the "processed data" of lines 4 and 5 would be serial, and that the "processed data" of lines 6 and 8 are parallel, therefore the meaning of processed data in the claim is indefinite.

12. Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The "serializer/deserializer" and "processed data" are each indefinite limitations for the same reasoning as presented above for Claims 1 and 12. The same serializer/deserializer of line 2 cannot be the serializer/deserializer of lines 5 and 8, and the same processed data of line 6 cannot be the processed data of lines 7 and 9.

13. Claim 21 recites the limitation "the transmitted data" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

14. Claims 1, 2, 5-7, 10-12, 14, 15, 18, 19, 21 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Takinosawa, U.S. Patent No. 6977960.

As per Claim 1:

Takinosawa teaches a built-in self-test circuit for testing a serializer/deserializer circuit (see Title) comprising: a transmit register (the pseudo-random shift register of column 5 lines 64-67 and column 6 lines 1-10 and FIG.4a 61) that transmits data (from the BIST 35 of FIG. 2) to the serializer/deserializer (FIG.2 39 and 46) for processing into processed data (serializing at 39 and deserializing at 46); a receive register that receives the processed data (FIG.2 48) from the serializer/deserializer; and an error detector (FIG.2 49 and FIG.4b 49) that detects errors in the processed data (FIG.4b Comparator 67 yields BIST_ERR), the transmit register (FIG.4a 61) being a programmable transmit register (via FIG.4a Data In 21, and Abstract) that transmits data having programmably varying characteristics (Summary, column 2 lines 35-46).

As per Claims 2 and 22:

Takinosawa further teaches the built-in self-test circuit of claim 1 or 21 wherein the programmably varying characteristics includes data sequence (data patterns of column 8 lines 21-32).

As per Claims 5 and 14:

Takinosawa further teaches the built-in self-test circuit of claim 1 or 12 wherein the programmable transmit register comprises a programmable bit sequence generator that generates the transmitted data (column 2 lines 35-46 and column 5 lines 64-67 and column 6 lines 1-10).

As per Claim 6:

Takinosawa further teaches the built-in self-test circuit of claim 1 wherein the programmable transmit register comprises a shift register (column 5 lines 64-67 and column 6 lines 1-10).

As per Claims 7, 15 and 19:

Takinosawa further teaches the built-in self-test circuit of claim 1 or 12 or 18 wherein the programmable transmit register comprises a pseudo random counter (column 5 lines 64-67 and column 6 lines 1-10).

As per Claim 10:

Takinosawa further teaches the built-in self-test circuit of claim 1 wherein the transmitted data and processed data are parallel data (the 16-bit data of FIG.2 35 and 49, and FIG.4a, 4b).

As per Claim 11:

Takinosawa further teaches the built-in self-test circuit of claim 1 wherein the error detector comprises a comparator (FIG.4b 67).

As per Claim 12:

Takinosawa teaches a built-in self-test circuit for testing a serializer/deserializer circuit comprising: a programmable transmit register (Abstract and Summary) that transmits data having programmably varying data sequences to the serializer/deserializer (column 2 lines 35-46 and column 5 lines 64-67 and column 6 lines 1-10) for processing into processed data (FIG.2 39 serializes and 46 deserializes); a receive register (FIG.2 48) that receives the processed data from the serializer/deserializer (column 5 lines 23-46); and an error detector that detects errors in the processed data (FIG.4b 67).

As per Claim 18:

Takinosawa teaches an integrated circuit (see Background) comprising: a serializer/deserializer circuit (FIG.2 39 and 46) that processes data (the serializer and deserializer data processes are well known); and a built-in self-test circuit (FIG.2 35) that includes, a programmable transmit register (FIG.4a 61) that transmits data having programmably varying characteristics to the serializer/deserializer circuit (column 2 lines 35-46 and column 5 lines 64-67 and column 6 lines 1-10) for processing into processed data (FIG.2 31 and 32); a receive register (FIG.2 48) that receives the processed data from the serializer/deserializer; and an error detector (FIG.4b 67) that detects errors in the processed data (BIST_ERR).

As per Claim 21:

Takinosawa teaches; in an integrated circuit, a method comprising: providing programmably varying data (Abstract, Summary) to a serializer/deserializer circuit (FIG.2 39, 46); processing the transmitted data with the serializer/deserializer circuit to produce processed data (the serializer and deserializer processes are well known); and testing the processed data for errors (FIG, 4b).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 3, 4, 13 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takinosawa, U.S. Patent No. 6977960 as applied to claims 1, 12 and 21 above, and further in view of Fan et al. (herein Fan), U.S. Patent Application No. 2004/0030968. Takinosawa further teaches the built-in self-test circuit of claim 1 or 12 or 21 wherein the programmably varying characteristics include data sequence but fails to disclose varying data length. But Fan does teach this feature in paragraph [0056]. And in paragraph [0015], the advantage stated is a means of counting errors in a self-test serial data transceiver at high data rates approaching 10 Gbps. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to apply the high speed test system of Fan (including the programmable

sequence length capability) with the slower system of Takinosawa in order to also test at high speeds.

16. Claims 8, 9, 16, 17, 20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takinosawa, U.S. Patent No. 6977960 as applied to claims 1, 12 and 21 above, and further in view of Chen et al. (herein Chen), U.S. Patent No. 5726991.
As per Claims 8, 9, 16, 17 and 20:

Although Takinosawa teaches a pseudo random counter, the reference fails to disclose a register array with pointer. But in the analogous art of Chen, this feature is disclosed in column 3 lines 65-67 and column 4 lines 1-20. Such a read only memory or register is well known in the art and would be considered as an array of registers. A counter or pointer would also be a well-known and obvious part of the data fetch in such a register. And Chen, in column 5 lines 26-32, an advantage is testing of where the transmitters and receivers are one unit, as in a PC. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to include with Takinosawa, features of Chen, including fixed pattern data in a read only memory or register, in order to provide test data for testing PC interfaces as well.
As per Claim 24:

Chen further teaches where Takinosawa fails, the method of claim 21 wherein the testing step includes comparing the provided data to the processed data. Such a feature is taught in column 5 lines 16-40, where the transmitter and receiver are integrated together, and control unit 34 and 58 become one, as well as pattern

generator 36 and 36A. The integrated package would thus use the same generator to generate data and to provide the comparison data, as is claimed in Claim 24. And in view of the motivation previously stated, the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2138

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